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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/851,943	05/10/2001	Yasuyuki Mishima	HITA.0053	4052

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Stanley P. Fisher
Reed Smith Hazel & Thomas LLP
3110 Fairview Park Drive, Suite 1400
Falls Church, VA 22042-4503

EXAMINER
KOVALICK, VINCENT E

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 03/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/851,943	MISHIMA ET AL.	
	Examiner	Art Unit	
	Vincent E Kovalick	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5 and 7-10* is/are rejected.

7)☒ Claim(s) *3 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This Office Action is in response to Applicant's Patent Application, Serial No. 09/851,942), with a File Date of May 10, 2001.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2 and 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al. (USP 6,320,630) taken with Asada et al. (USP 5,963,287) in view of Nomura (USP 6,448,810).

Relative to claim 1, Yamashita et al. **teaches** a Liquid Crystal Display device having slim driver chip (col. 1, lines 46-67; lines 1-67 and col. 3, lines 1-62); Yamashita et al. further **teaches** a Liquid Crystal Display (LCD) device comprising a liquid crystal display element and a plural driving circuits (col. 5, lines 13-20); a display control device which transmits display data and a clock signal to the plurality driving circuits (col. 6, lines 18-24).

Yamashita et al. **does not teach** a circuit board which is provided between the display control device and the plural driving circuits and supplies the display data and the clock signal transmitted from the display control device, to each of the driving circuits via a bus line and a

clock line in the circuit board, each of the bus line and the clock signal line of the circuit board being formed in a continuous area of the circuit board and being divided into plural lines.

Asada et al. **teaches** a Display Unit with Flexible Printed Circuit Board (col. 3, lines 28-67 and col. 4, lines 1-62); Asada et al. further **teaches** a circuit board which is provided between the display control device and the plural driving circuits and supplies the display data and the clock signal transmitted from the display control device, to each of the driving circuits via a bus line and a clock line in the circuit board (col. 7, lines 8-23), each of the bus line and the clock signal line of the circuit board being formed in a continuous area of the circuit board (col. 7, lines 9-14 and Fig. 4, items 55 and 56). It being obvious to a person of ordinary skill in the art at the time of the invention that a clock signal would have to be transmitted along with the data signals to be consistent with LCD data being transferred from display control means to the display device.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught by Yamashita et al. the feature as taught by Asada et al. in order to put in place the means to transfer the image data from the control logic to the image (LC D) display means.

Yamashita et al. taken with Asada et al. **does not teach** each of the bus line and the clock signal being divided into plural lines.

Nomura **teaches** a bidirectional bus-repeater controller (col. 2, lines 18-45); Nomura further **teaches** bus lines being divided into plural lines (col. 11, lines 20-31 and Fig. 11); it would have been obvious to a person of ordinary skill in the art at the time of the invention that the practice of dividing the bus lines would need to be applied to the associated clock signal lines as well.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught Yamashita et al. taken with Asada et al. the feature as taught by Nomura in order to incorporate the feature of dividing the bus and clock signal lines to reduce the generation of radiation electromagnetic noise being produced.

Regarding claims 2 and 5, Yamashita et al. **teaches** a said LCD wherein the display control device supplies the display data and the clock signal to each of the divided bus lines and clock signal lines in sequence in accordance with transmission timing (col. 6, lines 18-24). It would have been obvious to a person of ordinary skill in the art at the time of the invention that with the teaching of Yamashita et al. wherein a system computer (display control device) generates all the signals to drive the image display device, said computer would generate the data and clock signals to each of the divided bus lines and clock signal lines in sequence in accordance with transmission timing.

Relative to claim 4, Nomura **teaches** bus lines being divided into plural lines (col. 11, lines 20-31 and Fig. 11). It would have been obvious to a person or ordinary skill in the art at the time of the invention what with the means to divide bus lines and clock signal lines the division could be limited to just two lines.

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al. taken with Asada et al. in view of Nomura as applied to claim 4 in item 3 hereinabove, and further in view of Dong (USP 6,338,630).

Regarding claim 7, Yamashita et al. taken with Asada et al. in view of Nomura **does not teach** said LCD wherein a connector for inputting the display data and the clock signal from the display control device is provided in a lengthwise central portion of the circuit board.

Dong **teaches** a Board-to-Board Connector with improved contacts (col. 1, lines 32-63); Dong further **teaches** a connector for inputting the display data and the clock signal from the display control device is provided in a lengthwise central portion of the circuit board (col. 2, lines 17-24).

It would have been obvious to a person of ordinary skill in the at the time of the invention to incorporate in the device as taught by Yamashita et al. taken with Asada et al. in view of Nomura the feature as taught by Dong in order to optimize the data and clock signal flow to the bus lines, and/or the placement of the connector relative to a mating connection.

5. Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al. taken with Asada et al. in view of Nomura as applied to claim 4 in item 3 hereinabove, and further in view of Ode et al. (USP 6,518,946).

Regarding claim 8, Yamashita et al. taken with Asada et al. in view of Nomura **does not teach** said LCD wherein the clock signal is a clock signal for latching display data.

Ode **teaches** a liquid crystal display device (col. 2, lines 29-67 and col. 3, lines 1-27); Ode further **teaches** said LCD wherein the clock signal is a clock signal for latching display data (col. 5, lines 62-64).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught by Yamashita et al. taken with Asada et al. in view of Nomura the feature as taught by Ode in order to provide the means for latching the display data once said data was established for transmission to the display device.

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al. taken with Asada et al. in view of Nomura as applied to claim 1 in item 3 hereinabove, and further in view of Chiba et al. (USP 6,380,918).

Relative to claim 9, Yamashita et al. taken with Asada et al. in view of Nomura **does not teach** a connector for inputting the display data and the clock signal from the display control device being provided in a portion other than a lengthwise end portion of the circuit board.

Chiba et al. **teaches** a Liquid Crystal Display device (col. 3, lines 16-67; col. 4, lines 1-67 and col. 5, lines 1-36); Chiba et al. further **teaches** a connector for inputting the display data and the clock signal from the display control device being provided in a portion other than a lengthwise end portion of the circuit board (col. 2, lines 12-17 and Fig. 1, item 11).

It would have been obvious to a person of ordinary skill in the art at the time of the invention that the placement of the circuit board connector could be placed other than in a lengthwise end portion of the circuit board; or, in a lengthwise central portion of the circuit board which ever configuration would optimize the signal flow to the bus lines, and/or the placement of the connector relative the mating connection.

It would have further been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught by Yamashita et al. taken with Asada et al. in view of Nomura the feature as taught by Chiba et al in order to put in place the means to transmit the display data and the clock signals from the display control device to the display device.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al. taken with Asada et al. in view of Nomura and further in view of Chiba et al. as applied to claim 9 in item 6 hereinabove, and still further in view of Dong.

Regarding claim 10, Yamashita et al. taken with Asada et al. in view of Nomura and further in view of Chiba et al. **does not teach** said LCD wherein the connector is provided in a lengthwise central portion of the circuit board.

Dong **teaches** a connector for inputting the display data and the clock signal from the display control device is provided in a lengthwise central portion of the circuit board (col. 2, lines 17-24).

It would have been obvious to a person of ordinary skill in the at the time of the invention to incorporate in the device as taught by Yamashita et al. taken with Asada et al. in view of Nomura and still further in view of Chiba et al. the feature as taught by Dong in order to optimize the data and clock signal flow to the bus lines, and/or the placement of the connector relative to a mating connection.

Allowable Subject Matter

8. Claim 3 and 6 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claims 3 and 6, the major difference between the teachings of the prior art of record (USP 5,963,287, Asada et al.; USP 6,320,630, Yamashita et al. and USP 6,448,810, Nomura) is that said prior art **does not teach** an LCD wherein the display control device supplies a signal of

fixed voltage level to each of the divided bus lines and clock signal lines to which the display data and the clock signal are not supplied.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No.	6,518,946	Ode et al.
U. S. Patent No.	6,166,725	Isami et al.
U. S. Patent No.	6,023,310	Kawamoto et al.
U. S. Patent No.	4,492,460	Considine

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent E Kovalick whose telephone number is 703 306-3020. The examiner can normally be reached on Monday-Thursday 9:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703 305-4938. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872-9314 for regular communications and 703 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 306-0377.

Vincent E. Kovalick

February 28, 2003